SGS-THOMSON MICROELECTRONICS

QUALITY & RELIABILITY REPORT

Oct. 1994 to Sept. 1995 - EPROM, FLASH Memory, EEPROM and SRAM Products

INTRODUCTION

SGS-THOMSON manufactures a wide range of memory types which include:

Non-volatile memories: FLASH Memory, EPROM, OTP Memory and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; FLASH Memories in 1.2 to 0.6µ CMOS technology; OTP ROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Static RAMs: Fast SRAM, both Synchronous and Asynchronous and NVRAMs (ZEROPOWER and TIMEKEEPER ranges). Fast SRAMs are manufactured in 0.7-0.6µ HCMOS technology; NVRAMs in 1.2-0.8µ HCMOS.

Packages for Static RAM products include the plastic PDIP, PLCC and SOJ. Some of the ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional ”top hat” assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from October 1994 to September 1995. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Table 1. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	240	0	132	0	16,354	0	9,329	0	8,963	0	4,356	0
		– 168 hrs	240	0	132	0	2,133	0	1,287	0	1,068	0	2,580	0
		– 500 hrs	240	0	132	0	1,336	0	234	0	1,068	0	1,080	0
		– 1000 hrs	240	0	132	0	1,336	0	234	0	1,068	0	798	0
Retention Bake	1008	250°C,												
		– 48 hrs	200	0	200	0	1,400	0	400	0	500	0	1,100	0
		– 168 hrs	200	0	200	0	1,400	0	400	0	500	0	1,100	0
		– 500 hrs	200	0	200	0	1,400	0	400	0	500	0	1,100	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 2. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 2,207 375 375 375 -	 0 0 0 0 -
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs	 150 150 150	 0 0 0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 3. CMOS E5/0.8µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B (B) M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, (50% '0')		
		– 48 hrs	20,818	0
		– 168 hrs	425	0
		– 500 hrs	425	0
		– 1000 hrs	425	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C, (99% '0')		
		– 48 hrs	250	0
		– 168 hrs	250	0
		– 500 hrs	250	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 4. CMOS E5/0.8µm Process (-20% upgrade) UV EPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512 (C)		M27C1001 (C)		M27C1024 (B)		M27C2001 (C)		M27C4001 (D)		M27C4002 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	11,069	0	11,856	0	3,706	0	5,355	0	1,676	0	9,445	0
		– 168 hrs	1,592	0	1,773	1 (a)	242	0	275	0	522	0	168	0
		– 500 hrs	1,592	0	1,497	0	242	0	275	0	522	0	168	0
		– 1000 hrs	1,592	0	1,497	0	242	0	275	0	522	0	168	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	1,000	0	1,096	0	200	0	100	0	300	0	50	0
		– 168 hrs	1,000	0	1,096	0	200	0	100	0	300	0	50	0
		– 500 hrs	1,000	0	896	0	200	0	100	0	300	0	50	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
Fail a. Contact spiking (barrier defectivity)

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 5. CMOS E5/0.8μm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)		M27C801		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	9,310	0	4,647	0	8,992	0	9,888	0	2,978	0
		– 168 hrs	2,154	0	243	0	2,755	0	266	0	283	0
		– 500 hrs	309	0	243	0	889	0	266	0	283	0
		– 1000 hrs	309	0	243	0	889	0	266	0	283	0
		– 2000 hrs	96	0	144	0	96	0	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	1,000	0	150	0	1,400	0	100	0	100	0
		– 168 hrs	1,000	0	150	0	1,400	0	100	0	100	0
		– 500 hrs	1,000	0	150	0	1,296	0	100	0	100	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 6. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	3,460	0
		– 500 cycles	3,460	0
		– 1000 cycles	2,200	0
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		
Thermal Shock	1011	–55 to 125°C,		
		– 60 cycles	325	0
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		
Salt Atmosphere	1009	Test Condition A, 35°C	50	0
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	925	0
Resistance to Solvents	2015	4 Solvent Solutions	296	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	250	0
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Environmental Sequence:				
1. Thermal Shock	1011	–55 to 125°C, 15 cycles		
2. Temperature Cycling	1010	–65 to 150°C, 100 cycles	100	0
3. Moisture Resistance	1004	–10 to 65°C, RH = 90%, 10 cycles of 24hrs		
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		
Mechanical Sequence:				
1. Mechanical Shock	2002	Test Condition B		
2. Vibration Variable Frequency	2007	Test Condition A	150	0
3. Constant Acceleration	2001	Test Condition E		
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		
Temperature Cycling	1010	–65 to 150°C, 10 cycles		
Constant Acceleration	2001	Test Condition E	150	0
– Fine Leak	1014	Test Condition A1		
– Gross Leak	1014	Test Condition C1		

Table 7. CMOS E5/0.8µm Process (–10% Upgrade) OTP Memory Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	898	0
		– 500 hrs	898	0
		– 1000 hrs	898	0
		– 2000 hrs	240	0
Retention Bake	1008	150°C,		
		– 168 hrs	915	0
		– 500 hrs	915	0
		– 1000 hrs	915	0
		– 2000 hrs	217	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:
- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 8. CMOS E5/0.8µm Process (–10% Upgrade) OTP Memory Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 600 600 600 298	 0 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 531 531 531 139	 0 0 0 0
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 1,233 1,233 1,233 960	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 1,020 1,020 1,020	 0 0 0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	175	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	50	0
Resistance to Solvents	2015	4 Solvent Solutions	136	0

Table 9. CMOS E5/0.8µm Process (–20% Upgrade) OTP Memory Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz												
		– 168 hrs	432	0	388	0	322	0	178	0	340	0	484	0
		– 500 hrs	384	0	388	0	322	0	178	0	340	0	484	0
		– 1000 hrs	288	0	388	0	322	0	178	0	340	0	484	0
		– 2000 hrs	96	0	48	0	48	0	-	-	96	0	96	0
Retention Bake	1008	150°C,												
		– 168 hrs	540	0	450	0	405	0	130	0	380	0	610	0
		– 500 hrs	540	0	450	0	405	0	130	0	380	0	610	0
		– 1000 hrs	540	0	450	0	405	0	130	0	380	0	610	0
		– 2000 hrs	180	0	60	0	180	0	-	-	120	0	230	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 10. CMOS E5/0.8µm Process (–20% Upgrade) OTP Memory Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	450	0	350	0	415	0	45	0	400	0	425	0
		– 500 hrs	450	0	350	0	415	0	45	0	400	0	425	0
		– 1000 hrs	400	0	350	0	415	0	45	0	400	0	425	0
		– 2000 hrs	100	0	100	0	100	0	-	-	50	0	150	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,												
		– 48 hrs	250	0	112	0	224	0	48	0	145	0	198	0
		– 96 hrs	250	0	112	0	224	0	48	0	145	0	198	0
		– 168 hrs	250	0	112	0	224	0	48	0	145	0	198	0
		– 240 hrs	139	0	28	0	56	0	-	0	28	0	28	0
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	800	0	380	0	451	0	50	0	260	0	516	0
		– 96 hrs	800	0	380	0	451	0	50	0	260	0	516	0
		– 168 hrs	800	0	380	0	451	0	50	0	260	0	516	0
		– 240 hrs	800	0	380	0	451	0	50	0	260	0	360	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	600	0	400	0	425	0	25	0	240	0	420	0
		– 500 cycles	600	0	400	0	425	0	25	0	240	0	420	0
		– 1000 cycles	540	0	400	0	425	0	25	0	240	0	300	0
Solderability:														
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 385/0											
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 95/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 320/0											

Table 11. CMOS E5/0.8µm Process (–35% Upgrade) OTP Memory Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz						
		– 168 hrs	249	0	328	0	288	0
		– 500 hrs	249	0	328	0	288	0
		– 1000 hrs	249	0	328	0	192	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	220	0	260	0	300	0
		– 500 hrs	220	0	260	0	300	0
		– 1000 hrs	220	0	260	0	300	0
		– 2000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 12. CMOS E5/0.8µm Process (–35% Upgrade) OTP Memory Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	250	0	150	0	200	0
		– 500 hrs	250	0	150	0	200	0
		– 1000 hrs	250	0	150	0	150	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	55	0	-	-	168	0
		– 96 hrs	55	0	-	-	168	0
		– 168 hrs	55	0	-	-	168	0
		– 240 hrs	-	-	-	-	28	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	180	0	235	0	300	0
		– 96 hrs	180	0	235	0	300	0
		– 168 hrs	180	0	235	0	300	0
		– 240 hrs	180	0	-	-	300	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	180	0	215	0	360	0
		– 500 cycles	180	0	215	0	360	0
		– 1000 cycles	180	0	215	0	360	0
Solderability:								
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 345/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 150/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 184/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS T4/1.2µm Process FLASH Memory Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Operating Life Test [1]	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	47,136	0	82,546	0
		– 168 hrs	676	0	516	0
		– 500 hrs	676	0	516	0
		– 1000 hrs	676	0	516	0
		– 2000 hrs	240	0	268	0
Retention Bake [1]	1008	150°C,				
		– 168 hrs	698	0	1.202	0
		– 500 hrs	698	0	1,202	0
		– 1000 hrs	698	0	1,202	0
		– 2000 hrs	200	0	510	0
Write/Erase Cycling		1,000 cycles	5,850	0	19,133	2 (a)
		10,000 cycles	-	-	614	1 (b)
Retention Bake	1008	150°C, 36 hrs	5,850	0	19,133	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failures.
Fail b. Erasing Failure, single bit failures.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 14. CMOS T4/1.2µm Process FLASH Memory Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	798	0	495	0
		– 500 hrs	798	0	495	0
		– 1000 hrs	798	0	495	0
		– 2000 hrs	200	0	260	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	299	0	213	0
		– 96 hrs	299	0	213	0
		– 168 hrs	299	0	213	0
		– 240 hrs	138	0	81	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	520	0	340	0
		– 96 hrs	520	0	340	0
		– 168 hrs	520	0	340	0
		– 240 hrs	480	0	340	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	480	0	330	0
		– 500 cycles	480	0	330	0
		– 1000 cycles	450	0	330	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	25	0	25	0
		– 500 cycles	25	0	25	0
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 395/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 75/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 308/0			

Table 15. CMOS T5/0.8μm Process FLASH Memory Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Operating Life Test [1]	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	125,865	0	72,864	0
		– 168 hrs	1,256	0	144	0
		– 500 hrs	1,256	0	144	0
		– 1000 hrs	1,256	0	144	0
		– 2000 hrs	194	0	96	0
Retention Bake [1]	1008	150°C,				
		– 168 hrs	1,442	0	260	0
		– 500 hrs	1,442	0	260	0
		– 1000 hrs	1,442	0	260	0
		– 2000 hrs	444	0	100	0
Retention Bake	1008	250°C,				
		– 168 hrs	546	0	-	-
		– 500 hrs	546	0	-	-
		– 1000 hrs	263	0	-	-
		– 2000 hrs	263	0	-	-
Write/Erase Cycling		1,000 cycles	21,378	3 (a)	11,514	0
		10,000 cycles	939	4 (b)	81	0
Retention Bake	1008	150°C, 36 hrs	21,378	0	11,514	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.
Fail b. Erasing Failure, single bit failure.

Table 16. CMOS T5/0.8µm Process FLASH Memory Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	650	0	150	0
		– 500 hrs	650	0	150	0
		– 1000 hrs	650	0	150	0
		– 2000 hrs	150	0	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	333	0	110	0
		– 96 hrs	333	0	110	0
		– 168 hrs	333	0	110	0
		– 240 hrs	104	0	83	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	910	0	160	0
		– 96 hrs	910	0	160	0
		– 168 hrs	910	0	160	0
		– 240 hrs	860	0	160	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	870	0	120	0
		– 500 cycles	870	0	120	0
		– 1000 cycles	870	0	120	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	25	0	-	-
		– 500 cycles	25	0	-	-
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 475/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 253/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 296/0			

Table 17. CMOS T5/0.8μm Process (–20% upgrade) FLASH Memory Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test [1]	1005	140°C, V_{CC} = 6V, f = 500kHz, – 24 hrs – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 2,701 76 76 76 76	 0 0 0 0 0	 1,983 246 246 246 195	 0 0 0 0 0	 52,439 1,013 1,013 867 276	 0 0 0 0 0
Retention Bake [1]	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 50 50 50 50	 0 0 0 0	 100 100 100 100	 0 0 0 0	 858 858 608 413	 0 0 0 0
Retention Bake	1008	250°C, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 - - - -	 - - - -	 - - - -	 - - - -	 1,435 1,435 1,435 1,223	 0 0 0 0
Write/Erase Cycling		1,000 cycles 10,000 cycles	672 -	0 -	589 -	0 -	15,893 99	3 (a) 1 (b)
Retention Bake	1008	150°C, 36 hrs	672	0	589	0	15,893	0

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.
Fail b. Erasing Failure, single bit failure.

Table 18. CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	48	0	96	0	241	0
		– 500 hrs	48	0	96	0	241	0
		– 1000 hrs	48	0	96	0	241	0
		– 2000 hrs	48	0	96	0	132	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	44	0	88	0	241	0
		– 96 hrs	44	0	88	0	241	0
		– 168 hrs	44	0	88	0	241	0
		– 240 hrs	44	0	88	0	132	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	120	0	200	0	290	0
		– 96 hrs	120	0	200	0	290	0
		– 168 hrs	120	0	200	0	290	0
		– 240 hrs	120	0	200	0	290	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	96	0	128	0	500	0
		– 500 cycles	96	0	128	0	500	0
		– 1000 cycles	96	0	128	0	440	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	100	0
		– 500 cycles	-	-	-	-	75	0
Solderability:								
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 235/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 75/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 128/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19A. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	200	0	8,950	0	2,400	0	-	-
		– 168 hrs	100	0	1,950	0	400	0	-	-
		– 500 hrs	100	0	1,950	0	400	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	-	-	1,400	0	400	0	100	0
		– 500 hrs	-	-	1,400	0	400	0	100	0
		– 1000 hrs	-	-	1,400	0	400	0	100	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	1,300	0	400	0	50	0
		1,000,000 cycles	-	-	1,300	0	400	0	50	0
Retention Bake	1008	150°C, 168 hrs	-	-	1,300	0	400	0	50	0

Table 19B. CMOS F4/1.2μm Process EEPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,				
		– 24 hrs	78	0	11,000	0
		– 168 hrs	78	0	3,000	0
		– 500 hrs	78	0	3,000	0
		– 1000 hrs	-	-	-	-
Retention Bake	1008	150°C,				
		– 168 hrs	700	0	1,000	0
		– 500 hrs	700	0	1,000	0
		– 1000 hrs	550	0	1,000	0
		– 2000 hrs	-	-	-	-
Write/Erase Cycling		100,000 cycles	800	0	1,450	0
		1,000,000 cycles	-	-	1,350	0
Retention Bake	1008	150°C, 168 hrs	800	0	1,450	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164		M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	-	-	1,035	0	120	0	135	0	478	0	1,490	0
		– 500 hrs	-	-	1,035	0	120	0	135	0	478	0	1,490	0
		– 1000 hrs	-	-	1,035	0	120	0	135	0	478	0	1,490	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	50	0	1,850	0	350	0	700	0	1,363	0	1,050	0
		– 96 hrs	50	0	1,850	0	350	0	700	0	1,363	0	1,050	0
		– 168 hrs	50	0	1,850	0	350	0	700	0	1,363	0	1,050	0
		– 240 hrs	50	0	-	-	-	-	-	-	-	-	-	-
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	50	0	2,170	0	350	0	700	0	1,370	0	1,000	0
		– 200 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,												
		– 500 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Solderability:														
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 588/0											
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 488/0											
– PLCC Package			Cumulative Sample/Fail = 75/0											
– TSOP Package			Cumulative Sample/Fail = 75/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 120/0											
Resististance to Surface Mount:														
– SO Package			Cumulative Sample/Fail = 1,125/0											
– TSOP Package			Cumulative Sample/Fail = 95/0											

Table 21. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 168 hrs	-	-	300	0	49	0	224	0	72	0
		– 500 hrs	-	-	300	0	49	0	224	0	72	0
		– 1000 hrs	-	-	-	-	49	0	224	0	-	-
Retention Bake	1008	150°C,										
		– 168 hrs	-	-	-	-	-	-	-	-	60	0
		– 500 hrs	-	-	-	-	-	-	-	-	60	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	50	0	250	0	-	-	-	-	58	0
		1,000,000 cycles	-	-	250	0	-	-	-	-	58	0
Retention Bake	1008	150°C, 168 hrs	50	0	250	0	-	-	-	-	58	0

Table 22. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C02 ST24W02		ST24C04 ST24W04		ST24E32	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	-	-	-	-	80	0
		– 500 hrs	-	-	-	-	80	0
		– 1000 hrs	-	-	-	-	80	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	300	0	50	0	400	0
		– 96 hrs	300	0	50	0	400	0
		– 168 hrs	300	0	50	0	400	0
		– 240 hrs	300	0	50	0	400	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	300	0	-	-	300	0
		– 200 cycles	-	-	-	-	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability:								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = -/-					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 144/0					
– PLCC Package			Cumulative Sample/Fail = -/-					
– TSOP Package			Cumulative Sample/Fail = -/-					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 104/0					
Resististance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 150/0					
– TSOP Package			Cumulative Sample/Fail = -/-					

Table 23. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz – 168 hrs – 500 hrs – 1000 hrs	 462 462 462	 0 0 0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 24. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 616 616 616	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 615 615	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 96/0	

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 25. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1KHz – 168 hrs – 500 hrs – 1000 hrs	 254 254 254	 0 0 0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 26. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 346 346 346	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 343 343	 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs	 - -	 - -
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 108/0	

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 27. HCMOS 4P/0.7µm Process SRAM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz – 168 hrs – 500 hrs – 1000 hrs	 1,752 506 506	 2 (a) 0 3 (b)

Notes: Fail a. Single bit and functional fail due to suspected particles. Multiple process improvements have been implemented to address polysilicon particle reduction, and have been verified to reduce defects.
Fail b. Single bit, Pattern fail, and speed fail due to suspected particles.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 28. HCMOS 4P/0.7µm Process SRAM Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 231 231 231	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 55 -	 0 -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 411 411	 0 1 (c)
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	

Note: Fail c. Functional fail due to suspected particles.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 29. HCMOS 4PS/0.6µm Process SRAM Reliability Data, Die Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628032	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz – 168 hrs – 500 hrs – 1000 hrs	 2,043 616 616	 2 (a) 0 0

Note: Fail a. Single bit failure due to particle at poly 2. Multiple process improvements have been implemented to address polysilicon particle reduction, and have been verified to reduce defects. Speed downgrade resulting in column block fail. No defects were found during deprocessing.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 30. HCMOS 4PS/0.6μm Process SRAM Reliability Data, Package Related Tests, Oct. 1994 to Sept. 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628032	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 77 77 77	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 45 -	 0 -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 163 163	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

STATISTICAL PROCESS CONTROL

NMOS E3/1.5μm Process UV EPROM, Rousset - France Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Gate Oxide Thickness	1.34	1.29	1.25	1.04	2.38	2.22	1.41	1.22
Interpoly Oxide Thickness (1)	2.05	1.11	1.53	1.45	2.06	1.80	1.08	1.06
Field Oxide Thickness	1.78	1.59	1.68	1.52	2.48	2.46	1.84	1.82
Intermediate Dielectric Thickness	4.52	4.40	7.28	7.02	5.31	5.11	3.01	2.76
Final P-Vapox Thickness	6.06	4.90	3.99	3.76	4.30	4.23	4.61	4.15
Polysilicon I Thickness	2.82	2.77	1.43	1.39	1.97	1.71	2.19	2.10
Polysilicon II Thickness	2.47	2.36	1.89	1.82	2.30	2.12	2.53	2.42
Aluminium 1% Si Thickness (SP1)	2.31	2.18	2.09	1.97	2.95	2.74	2.45	2.35
Polysilicon II Critical Dimensions	1.88	1.55	2.20	1.80	2.21	1.91	1.53	1.45
Active Area Critical Dimensions	3.67	3.13	1.44	1.36	3.18	3.13	2.61	2.15

Note: 1. To redefine the way to proceed, in the case of restart of recipe on a furnace.

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT Henancement 25 x 25 μm	2.17	2.13	2.98	2.78	2.46	2.46	2.28	2.27
VT Array 25 x 25 μm	2.85	2.45	4.50	4.06	4.25	3.75	2.96	2.69
VT Field	7.83	3.77	11.80	5.12	5.13	2.52	8.65	3.62
I_{DON} Depletion 25 x 25 μm	2.35	2.12	2.94	2.71	3.13	2.77	2.51	1.79
Polysilicon II Sheet Resistance	13.30	3.58	13.30	3.47	13.50	3.55	12.60	3.29
Buried Contact Chain Resistance	25.10	4.88	36.60	6.85	34.50	6.49	29.00	5.31
N+ Sheet Resistance	7.77	6.39	3.07	2.59	8.98	7.23	2.11	1.77
AL-Polysilicon II Contact Chain Resistance	9.91	4.55	12.80	5.74	10.80	5.07	10.50	4.84
AL-N+ Contact Chain Resistance	6.52	5.29	7.64	6.26	7.76	6.33	2.54	2.15

STATISTICAL PROCESS CONTROL

CMOS E5/0.8µm Process UV EPROM, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.20	2.27	2.26	2.20	2.23	2.22	3.17	3.10
Silicon Nitride Thickness	1.54	1.52	2.00	1.96	2.01	1.99	2.03	2.02
Field Oxide Thickness	1.51	1.41	1.37	1.34	1.41	1.40	1.85	1.81
Gate Oxide Thickness	2.32	2.31	2.02	1.89	2.01	1.95	2.34	2.24
Interpoly Oxide Thickness	1.60	1.59	1.59	1.57	1.90	1.82	1.67	1.56
Intermediate Dielectric Thickness	2.48	2.35	1.79	1.76	2.08	2.02	2.08	1.99
Polysilicon I Thickness	1.41	1.36	1.65	1.60	1.72	1.64	2.17	2.14
Active Area Critical Dimensions	2.75	2.32	1.97	1.74	1.94	1.69	3.24	3.15
Policide Critical Dimensions	2.45	2.26	1.80	1.62	1.53	1.41	2.46	2.27

Note: No UV EPROM wafer production in 3Q95.

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	3.23	2.71	4.66	4.03	2.55	2.19	2.53	2.38
VT P-Channel 25 x 25 µm	2.27	2.00	2.04	1.86	2.58	2.14	2.00	1.54
VT Natural 25 x 25 µm	4.57	4.16	3.92	3.54	4.25	3.91	4.37	4.21
VT Memory Cell 0.8 x 0.8 µm	1.91	1.86	1.97	1.63	1.66	1.64	1.72	1.70
I_{DON} N-Channel 25 x 0.8 µm	3.40	2.84	3.23	3.05	3.10	2.98	3.12	2.90
N+ Active Area Contact Chain	4.42	3.36	3.82	3.35	5.73	4.46	7.07	5.39
AL-Tungsten Silicide Contact Chain Resistance	4.36	2.85	2.87	2.49	2.04	1.77	3.01	2.47

STATISTICAL PROCESS CONTROL

CMOS E5/0.8µm Process UV EPROM and OTP Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.73	1.70	1.65	1.56	1.78	1.68	1.74	1.67
Silicon Nitride Thickness	1.57	1.40	1.50	1.34	1.47	1.41	1.48	1.46
Field Oxide Thickness	2.03	2.00	1.65	1.65	2.53	2.22	1.57	1.48
Gate Oxide Thickness	1.48	1.48	1.35	1.29	1.44	1.43	1.44	1.44
Interpoly Oxide Thickness	1.38	1.36	1.61	1.51	1.37	1.34	1.47	1.34
Intermediate Dielectric Thickness	1.81	1.59	1.85	1.81	1.75	1.68	1.91	1.83
Polysilicon I Thickness	2.98	2.96	2.80	2.74	2.63	2.58	2.91	2.90
Active Area Critical Dimensions	2.29	2.28	2.10	2.00	1.59	1.37	1.67	1.51
Policide Critical Dimensions	1.63	1.45	1.70	1.70	1.72	1.67	1.76	1.68

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.09	1.60	2.06	1.52	2.96	2.41	2.06	1.84
VT P-Channel 25 x 25 µm	2.20	1.77	2.70	2.24	3.28	3.22	2.53	2.56
VT Natural 25 x 25 µm	3.14	2.69	2.15	1.99	2.75	2.67	2.93	2.65
VT Memory Cell 0.8 x 0.8 µm	1.27	1.21	1.32	1.15	1.32	1.30	1.30	1.28
I_{DON} N-Channel 25 x 0.8 µm	1.84	1.73	2.02	1.94	2.52	2.39	2.00	1.84
N+ Active Area Contact Chain	4.51	3.87	6.04	5.29	4.39	3.78	4.60	4.19
AL-W Silicide Contact Chain Resistance	4.26	2.40	1.37	1.32	1.56	1.47	3.34	2.75

STATISTICAL PROCESS CONTROL

CMOS T4/1.2μm Process FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.51	1.50	1.37	1.35	1.41	1.40	1.85	1.81
Polysilicon I Thickness	1.41	1.36	1.65	1.60	1.72	1.64	2.17	2.14
Gate Oxide Thickness	2.30	2.25	2.10	2.10	2.12	2.06	2.06	1.99
Tunnel Oxide Thickness	1.47	1.44	1.42	1.39	1.43	1.41	1.84	1.83
ONO Bottom Oxide Thickness	1.32	1.29	1.74	1.40	1.58	1.57	1.40	1.36
ONO Nitride Thickness	1.24	1.20	1.34	1.30	1.26	1.25	1.47	1.44
ONO Top Oxide Thickness	2.10	2.10	2.21	2.19	1.96	1.93	2.25	2.23
Active Area Critical Dimensions	1.45	1.43	1.97	1.45	1.56	1.54	1.65	1.54
Polysilicon II Critical Dimensions	1.43	1.37	1.80	1.60	1.54	1.52	1.69	1.64

Note: No T4 FLASH Memory wafer production in 3Q95.

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 μm	3.64	3.00	2.67	2.09	2.24	2.22	1.88	1.80
VT P-Channel 25 x 25 μm	1.74	1.72	1.74	1.43	1.92	1.85	1.72	1.68
BV N-Channel 25 x 1.2 μm	1.56	1.43	1.45	1.41	1.44	1.41	1.44	1.39
BV P-Channel 25 x 1.6 μm	6.78	4.51	4.34	3.95	3.97	3.95	5.97	5.71
VT Memory Cell 0.8 x 0.8 μm	1.78	1.41	1.39	1.37	1.20	1.18	1.50	1.38
I_{DON} N-Channel 25 x 1.2 μm	1.80	1.67	2.04	1.34	1.78	1.78	1.71	1.70
Al-N+ Contact Chain	1.47	1.25	1.51	1.36	1.35	1.34	1.36	1.34
AL-W Silicide Contact Chain Resistance	1.54	1.48	1.53	1.45	1.45	1.43	1.65	1.63

STATISTICAL PROCESS CONTROL

CMOS T5/0.8μm Process FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.37	1.35	1.41	1.40	1.85	1.81	2.01	1.96
Polysilicon I Thickness	1.65	1.60	1.72	1.64	2.17	2.14	1.45	1.42
Gate Oxide Thickness	2.10	2.10	2.12	2.06	2.06	1.99	3.07	3.03
Tunnel Oxide Thickness	1.42	1.39	1.43	1.41	1.84	1.83	2.39	2.38
ONO Bottom Oxide Thickness	1.74	1.40	1.58	1.57	1.40	1.36	1.57	1.49
ONO Nitride Thickness	1.34	1.30	1.26	1.25	1.47	1.44	1.50	1.44
ONO Top Oxide Thickness	2.21	2.19	1.96	1.93	2.25	2.23	1.60	1.59
Active Area Critical Dimensions	1.83	1.40	1.44	1.42	1.65	1.59	2.39	2.31
Polysilicon II Critical Dimensions	1.62	1.39	1.18 (1)	0.87	1.35	1.29	2.07	1.89

Note: 1. Low CPK is due to change of dimensional target to improve the access time.

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 μm	2.38	1.81	2.80	2.79	1.69	1.55	1.56	1.50
VT P-Channel 25 x 25 μm	2.27	2.01	1.89	1.77	1.15 (1)	1.04 (1)	1.46	1.43
BV N-Channel 25 x 1.2 μm	4.54	3.90	4.59	4.59	3.56	3.48	1.44	1.41
BV P-Channel 25 x 1.6 μm	2.86	2.61	5.70	5.64	2.96	2.87	1.68	1.54
VT Memory Cell 0.8 x 0.8 μm	1.88	1.71	2.10	2.04	1.91	1.83	1.56	1.51
I_{DON} N-Channel 25 x 1.2 μm	2.24	1.84	2.24	2.14	1.45	1.34	1.78	1.75
Al-N+ Contact Chain	4.59	4.15	2.89	2.80	3.78	3.64	4.30	4.25
Al-W Silicide Contact Chain Resistance	2.56	2.50	2.62	2.60	4.45	4.36	2.05	1.94

Note: 1. Some runs with high variability of this parameter on furnace 5. A specific analysis is running.

STATISTICAL PROCESS CONTROL

CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 95							
	CP	CPK						
Field Oxide Thickness	2.01	1.96						
Polysilicon I Thickness	1.45	1.42						
Gate Oxide Thickness	3.07	3.03						
Tunnel Oxide Thickness	2.39	2.38						
ONO Bottom Oxide Thickness	1.57	1.49						
ONO Nitride Thickness	1.50	1.44						
ONO Top Oxide Thickness	1.60	1.59						
Active Area Critical Dimensions	1.83	1.65						
Polysilicon II Critical Dimensions	1.95	1.88						

Key Electrical Parameters	3Q 95							
	CP	CPK						
VT N-Channel 25 x 25 µm	1.59	1.44						
VT P-Channel 25 x 25 µm	1.54	1.45						
BV N-Channel 25 x 1.2 µm	3.69	3.38						
BV P-Channel 25 x 1.6 µm	2.30	2.26						
VT Memory Cell 0.8 x 0.8 µm	1.65	1.61						
I_{DON} N-Channel 25 x 1.2 µm	1.92	1.88						
Al-N+ Contact Chain	3.88	3.81						
Al-W Silicide Contact Chain Resistance	2.55	2.51						

STATISTICAL PROCESS CONTROL

UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Shear Test (D.A.)	(*)	5.00	(*)	3.66	(*)	2.82	(*)	3.25
Bond Strength (W.B.)	(*)	2.77	(*)	2.59	(*)	2.51	(*)	2.55
SN Thickness (Tin Plate)	1.70	1.85	1.62	1.43	1.56	1.43	1.56	1.50
Lead Lenght (Cropping)	2.00	2.80	1.78	2.66	3.67	2.20	4.47	3.37

Note: *. One side limit only (CPL).

FAILURE RATE PREDICTIONS

October 1994 to September 1995

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -20%	6.19	140	0.6	4.0	1,694	1	1.2	2.3
CMOS E5 -35%	4.39	140	0.6	4.0	1,206	0	0.8	1.9
NMOS E3	6.05	140	0.6	2.6	782	0	1.2	2.9
OTP								
CMOS E5 -20%	2.44	140	0.6	4.0	632	0	1.4	3.6
CMOS E5 -35%	0.81	140	0.6	4.0	212	0	4.3	11.0
FLASH								
CMOS T4	4.78	140	0.6	3.0	930	0	1.0	2.5
CMOS T5	6.42	140	0.6	4.0	1,665	0	0.5	1.4
CMOS T5 -20%	3.15	140	0.6	4.0	816	0	1.1	2.8
SRAM								
CMOS Spectrum	0.46	125	0.7	4.0	142	0	6.4	16.0
HCMOS S3	0.25	125	0.7	4.0	78	0	11.0	29.0
HCMOS 4P	0.72	125	0.7	5.7	315	5	20.0	29.0
HCMOS 4PS	0.86	125	0.7	5.7	376	2	8.3	14.0
EEPROM								
CMOS F4	3.20	140	0.6	3.0	746	0	1.2	3.0

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